

ABSTRACT OF THE DISCLOSURE

A semiconductor storage device comprises a memory cell array including memory cells, and bit lines for transfer of data in the memory cells; an amplifier
5 circuit connected to the bit lines to amplify data in the memory cells; a first switching element connected between the bit lines and the amplifier circuit; a first reference voltage source which applies to the gate of the first switching element a voltage for turning the
10 first switching element ON; a second switching element and a third switching element connected in series between the gate of the first switching element and the first reference voltage source, said second switching element and said third switching element being connected
15 in parallel to each other; a second reference voltage source which applies to the gates of the second and third switching elements a voltage for turning the second and third switching elements ON; and a first timing shift circuit connected between the gate of the
20 third switching element and the second reference voltage source to delay the operation of the third switching element from the operation of the second switching element.